Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1 (currently amended): A method for pre-fetching data from a memory, comprising the steps of:

initializing a counter value;

pre-fetching a predetermined data from the memory and subtracting a first value from the counter value ~~when a~~ each time pre-fetching is activated;

adding a second value to the counter value when a cache hit occurs;

comparing the counter value with a first threshold value; and

when the counter value is smaller than the first threshold value, stopping pre-fetching data from the memory.

2 (original): The method of claim 1, wherein when the pre-fetching is stopped, the counter value is blocked from being decreased by the first value.

3 (original): The method of claim 2, wherein when the pre-fetching is stopped and the cache hit occurs, the second value is added to the counter value.

4 (original): The method of claim 3, wherein when the pre-fetching is stopped and the counter value is larger than a second threshold value, pre-fetching data from the memory is restarted.

5 (original): The method of claim 4, wherein the second threshold value is larger than the first threshold value.

6 (original): The method of claim 1, wherein the second value is an integer multiple of the

first value.

7 (currently amended): A method for pre-fetching data from a memory, comprising the steps of:

initializing a counter value;

pre-fetching a predetermined data from the memory and adding a first value to the counter value ~~when a~~ each time pre-fetching is activated;

subtracting a second value from the counter value when a cache hit occurs;

comparing the counter value with a first threshold value; and

when the counter value is larger than the first threshold value, stopping pre-fetching data from the memory.

8 (original): The method of claim 7, wherein when the pre-fetching is stopped, the counter value is blocked from being increased by the first value.

9 (original): The method of claim 8, wherein when the pre-fetching is stopped and the cache hit occurs, the counter value is decreased by the second value.

10 (original): The method of claim 9, wherein when the pre-fetching is stopped and the counter value is smaller than a second threshold value, pre-fetching data from the memory is restarted.

11 (original): The method of claim 10, wherein the second threshold value is smaller than the first threshold value.

12 (original): The method of claim 7, wherein the second value is an integer multiple of the first value.

13 (currently amended): A pre-fetch controller for pre-fetching data from a memory for a logic operation unit, the pre-fetching controller comprising:

a register for storing a counter value; and

a controller electrically connected to the register for changing the counter value ~~when a~~ each time pre-fetching is activated [[or]] and when a cache hit occurs.

14 (original): The pre-fetch controller of claim 13, wherein the controller further comprises an operating unit for predicting a predetermined data required by the logic operation unit and pre-fetching the predetermined data from the memory when the pre-fetching is activated.

15 (original): The pre-fetch controller of claim 13, wherein the controller further comprises an output unit for decreasing the counter value by a first value when the pre-fetching is activated.

16 (original): The pre-fetch controller of claim 15, wherein the controller further comprises a detecting unit for adding a second value to the counter value when the cache hit occurs.

17 (original): The pre-fetch controller of claim 16, wherein the second value is an integer multiple of the first value.

18 (original): The pre-fetch controller of claim 15, wherein the pre-fetch controller further comprises a comparing module electrically connected between the register and the controller for stopping pre-fetching data from the memory when the counter value becomes smaller than a first threshold value and for restarting pre-fetching data from the memory when the counter value becomes larger than a second threshold value after the pre-fetching is stopped.

19 (original): The pre-fetch controller of claim 18, wherein the counter value is blocked from being decreased by the first value when the pre-fetching is stopped, and the second value is added to the counter value when the pre-fetching is stopped and the cache hit occurs.

20 (original): The pre-fetch controller of claim 18, wherein the second threshold value is larger than the first threshold value.

21 (original): The pre-fetch controller of claim 13, wherein the controller further comprises an output unit for adding a third value to the counter value when the pre-fetching is activated.

22 (original): The pre-fetch controller of claim 21, wherein the controller further comprises a detecting unit for subtracting a fourth value from the counter value when the cache hit occurs.

23 (original): The pre-fetch controller of claim 22, wherein the fourth value is an integer multiple of the third value.

24 (original): The pre-fetch controller of claim 22, wherein the pre-fetch controller further comprises a comparing module electrically connected between the register and the controller for stopping pre-fetching data from the memory when the counter value becomes larger than a third threshold value and for restarting pre-fetching data from the memory when the counter value becomes smaller than a fourth threshold value after the pre-fetching is stopped.

25 (original): The pre-fetch controller of claim 24, wherein the third value is blocked

from being added to the counter value when the pre-fetching is stopped, and the fourth value is subtracted from the counter value when the pre-fetching is stopped and the cache hit occurs.

26 (currently amended): The pre-fetch controller of claim 22, wherein the fourth ~~threshold~~ value is smaller than the third ~~threshold~~ value.

27 (original): The pre-fetch controller of claim 13, wherein the pre-fetch controller further comprises a subtractor electrically connected to the register for changing the counter value.

28 (original): The pre-fetch controller of claim 13, wherein the pre-fetch controller further comprises an adder electrically connected to the register for changing the counter value.

29 (currently amended): A data processing device for pre-fetching data from a memory and providing data to a logic operation unit, the data processing device comprising:

a first memory for storing prediction data;

a second memory for storing data and providing the logic operation unit with data;

a memory controller electrically connected to the second memory for pre-fetching data from the second memory to the first memory; and

a pre-fetch controller, electrically connected between the second memory and the memory controller, for predicting a data required by the logic operating unit and controlling the memory controller to pre-fetch the data from the second memory, wherein the pre-fetch controller has a counter value, compares the counter value with a first threshold value to determine whether to stop a pre-fetching for data in the second memory, and compares the counter value with a second threshold value to determine whether to restart pre-fetching data from the second memory after the pre-fetching is stopped,

wherein the counter value is changed each time pre-fetching is performed and when a cache hit occurs.

30 (original): The data processing device of claim 29, wherein the pre-fetching controller comprises:

a register for storing the counter value; and

a comparing module electrically connected to the register for comparing the counter value with a first threshold value and a second threshold value.

31 (original): The data processing device of claim 30, wherein the pre-fetching controller further comprises a controller electrically connected to the comparing module for changing the counter value when the pre-fetching is activated and the cache hit occurs.

32 (original): The data processing device of claim 31, wherein the controller comprises:

an operating unit for predicting the data required by the logic operating unit and controlling the memory controller to fetch the data from the second memory;

an output unit for sending a first command when the pre-fetching is activated; and

a detecting unit for sending a second command when the cache hit occurs.

33 (original): The data processing device of claim 32, wherein the counter value is decreased by a first value when the pre-fetching is performed, and the counter value is increased by a second value when the cache hit occurs.

34 (original): The data processing device of claim 33, wherein the second value is an integer multiple of the first value.

35 (original): The data processing device of claim 34, wherein the pre-fetching is stopped when the counter value becomes smaller than the first threshold value, and the

pre-fetching is restarted when the counter value becomes larger than the second threshold value.

36 (original): The data processing device of claim 35, wherein the second threshold value is larger than the first threshold value.

37 (original): The data processing device of claim 32, wherein a third value is added to the counter value when the pre-fetching is activated, and a fourth value is subtracted from the counter value when the cache hit occurs.

38 (original): The data processing device of claim 37, wherein the fourth value is an integer multiple of the third value.

39 (currently amended): The data processing device of claim 37, wherein pre-fetching data from the second memory is stopped when the counter value becomes larger than the third ~~threshold~~ value, and pre-fetching data from the second memory is restarted when the counter value becomes smaller than the fourth ~~threshold~~ value.

40 (currently amended): The data processing device of claim 39, wherein the fourth ~~threshold~~ value is smaller than the third ~~threshold~~ value.

41 (original): The data processing device of claim 30, wherein the data processing device further comprises an adder electrically connected to the register for increasing the counter value.

42 (original): The data processing device of claim 30, wherein the data processing device further comprises a subtractor electrically connected to the register for decreasing the counter value by a first value or a second value.